3A, 23V, 340KHz Synchronous Step-Down Converter

General Description

The FP6193 is a synchronous buck regulator with integrated two 85mΩ power MOSFETs. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. The device includes cycle-by-cycle current limiting and thermal shutdown protection. The regulator only consumes 1μA supply current in shutdown mode. The FP6193 requires a minimum number of readily available external components to complete a 3A buck regulator solution.

Features

➢ 3A Output Current

➢ 85mΩ Internal Power MOSFET Switches

➢ Stable with Low ESR Output Ceramic Capacitors Up to 93% Efficiency

➢ 1μA Shutdown Mode Current

➢ Programmable Soft-Start

➢ Fixed 340KHz Frequency

➢ Thermal Shutdown

➢ Cycle-by-Cycle Over Current Protection

➢ Wide 4.75V to 23V Operating Input Range

➢ Output Adjustable From 0.923V to 20V

➢ Available SOP-8L (EP) Package
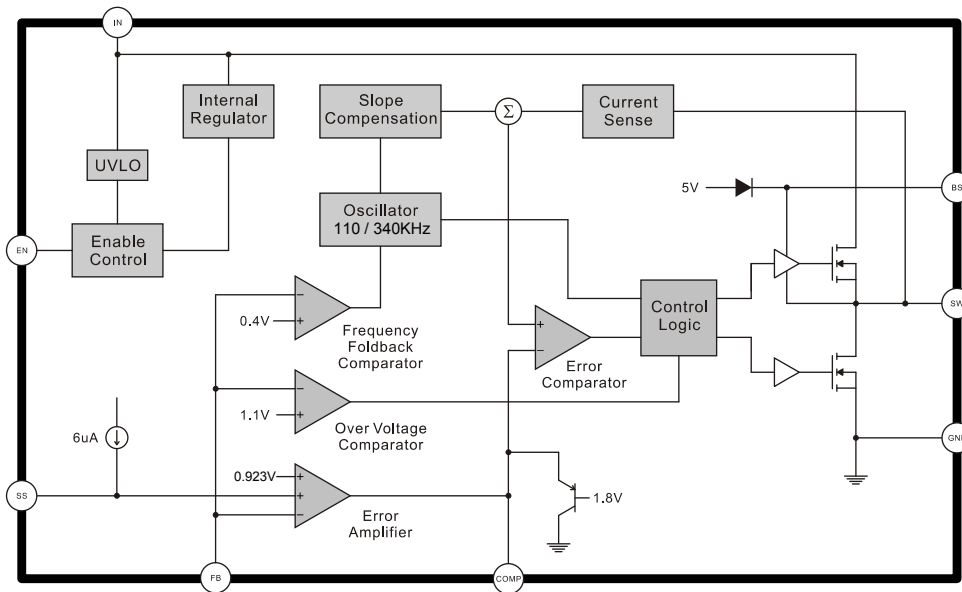
➢ Input Under Voltage Lockout

Applications

➢ Distributed Power Systems

➢ Battery Charger Network Cards

➢ Pre-Regulator for Linear Regulators

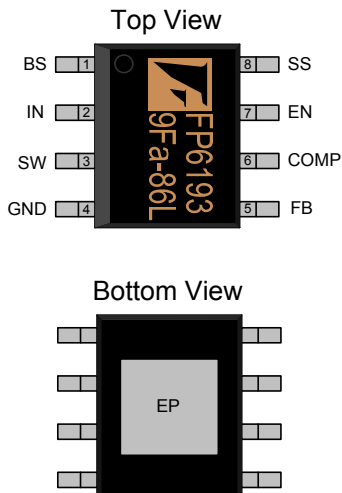➢ DSL Modems

Typical Application Circuit
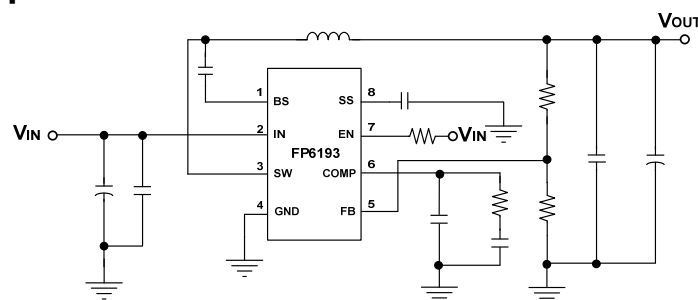
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Function Block Diagram

Pin Descriptions

SOP-8L (EP)

Top View

Bottom View

Name	No.	I / O	Description
BS	1	O	Bootstrap
IN	2	P	Supply Voltage
SW	3	O	Switch
GND	4	P	Ground
FB	5	I	Feedback
COMP	6	O	Compensation
EN	7	I	Enable / UVLO
SS	8	O	Soft-Start
EP	9	P	Exposed PAD is GND

Marking Information

SOP-8L (EP)
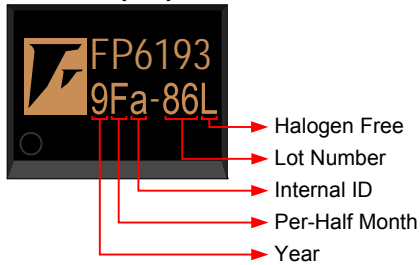
Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

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Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP6193XR-G1	-40°C ~ +85°C	SOP-8L (EP)	2500EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}		-0.3		24	V
Supply Voltage	V_{sw}		-1		V_{IN} +0.3	V
Bootstrap Voltage	V_{BS}		V_{sw} -0.3		V_{sw} +6	V
All Other Pins			-0.3		6	V
Junction Temperature	T_J				+150	°C
Storage Temperature	T_S		-65		+150	°C
Allowable Power Dissipation		SOP-8L (EP)			650	mW
Thermal Resistance	θ_{JA}	SOP-8L (EP)			+60	°C / W
	θ_{JC}				+10	°C / W
Lead Temperature (soldering, 10 sec)		SOP 8L (EP)		+260		°C

IR Re-flow Soldering Curve
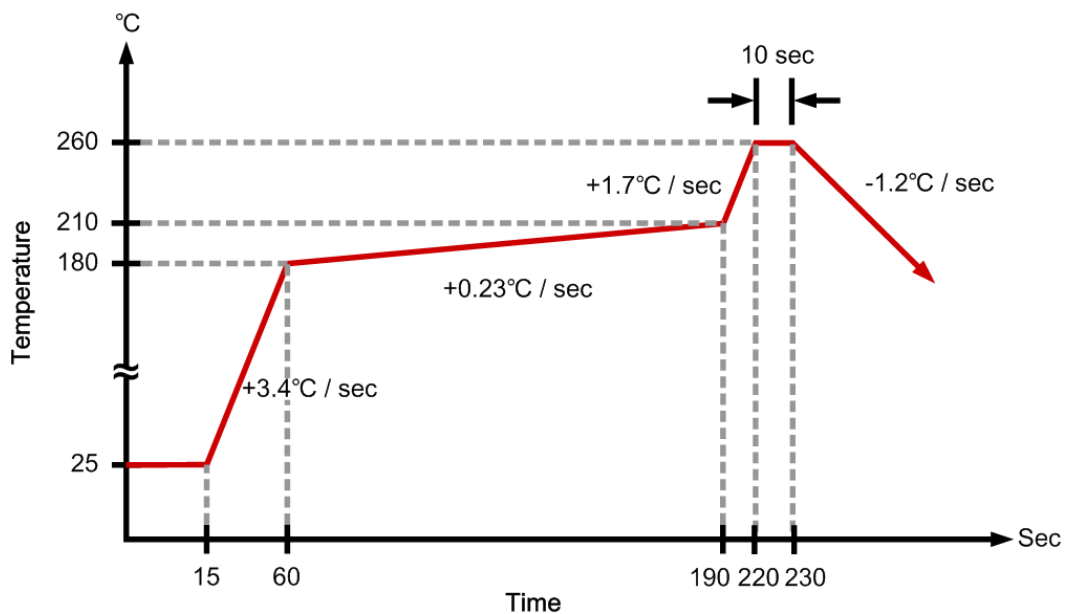
Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}		4.75		23	V
Operating Temperature			-40		+85	℃

DC Electrical Characteristics $(T_A$= 25℃, V_{IN}=12V, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Standby Current	I_{SB}	$V_{EN} \geq 3V, V_{FB} \geq 1.0V$		1.0	1.5	mA
Shutdown Supply Current	I_{ST}	$V_{EN}=0$		1	3	µA
Feedback Voltage	V_{FB}	V_{IN}=12V,V_{COMP}<2V	0.900	0.923	0.946	V
Feedback Over Voltage Threshold				1.1		V
Error Amplifier Voltage Gain	G_{EA}			400		V / V
Error Amplifier Transconductance	T_{EA}	$\triangle IC=\pm10µA$		830		µA / V
High Side Switch ON Resistance	R_{ON-HS}			85		mΩ
Low Side Switch ON Resistance	R_{ON-LS}			85		mΩ
High Side Switch Leakage Current	I_{IL}	$V_{EN}=0,V_{SW}=0V$		0.1	10	µA
High Side Current Limit	I_{HCL}		3.8	5.3		A
Low Side Current Limit	I_{LCL}	From Drain to Source		1		A
COMP to Current Sense Transconductance	T_{CS}			5.2		A / V
Oscillation Frequency	F_{OSC}			340		KHz
Short Circuit Oscillation Frequency	F_{SC}	$V_{FB}=0V$		110		KHz
Maximum Duty Cycle	D_{MAX}	$V_{FB}=0.8V$		90		%
Minimum On Time	T_{ON}			220		ns
Input Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	3.8	4.1	4.4	V
Input Under Voltage Lockout Threshold Hysteresis				200		mV
EN Lockout Threshold	V_{ENLO}	V_{EN} Rising	2.2	2.5	2.7	V
EN Lockout Threshold Hysteresis				250		mV
EN Threshold Voltage	V_{EN}		1.0	1.5	2.0	V
EN Threshold Voltage Hysteresis				300		mV
Soft-Start Current		$V_{SS}=0V$		6		µA
Soft start Period		$C_{SS}=0.1µF$		15		ms
Thermal Shutdown	T_{TS}			+150		℃

Function Description

The FP6193 is a synchronous current-mode buck regulator. It regulates input voltages from 4.75V to 23V down to an output voltage as low as 0.923V, and is able to supply up to 3A of load current. The FP6193 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified by the internal error amplifier. The output current of the trancondutance error amplifier is presented at COMP where a network compensates the regulation control system. The voltage at COMP is compared to the switch current measured internally to control the output voltage. The converter uses internal n-channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS drives the gate. The capacitor is charged from the internal regulator when the SW pin is low.

Output Voltage (V_{OUT})

The output voltage is set using a resistive voltage divider from the output voltage to FB. The voltage divider divides the output voltage down by the ratio:

$$V_{FB} = V_{OUT} \times \frac{R_4}{R_2 + R_4}$$

Thus the output voltage is:

$$V_{OUT} = V_{FB} \times \frac{R_2 + R_4}{R_4}$$

A typical value for R4 can be as high as 100KΩ, but a typical value is 10KΩ.

Enable Mode / Shutdown Mode

Drive the EN Pin to ground to shutdown the FP6193. Shutdown forces the internal power MOSFETs off, turns off all internal circuitry, and reduces the V_{IN} supply current to 1μA (typ). The EN Pin rising threshold is 1.5V (typ), and hysteresis is 300mV. For automatic startup application, pull up the EN pin with 100KΩ resister.

Boost High-Side Gate Drive (BST)

Since the MOSFET requires a gate voltage greater than the input voltage, connect a flying bootstrap capacitor between SW and BS to provide the gate-drive voltage to the high-side n-channel MOSFET switch. The capacitor is alternately charged from the internal regulator. On startup, an internal low-side switch connects SW to ground and charges the BST capacitor to internal regulated voltage. Once the BST capacitor is charged, and the internal low-side switch is turned off, the BST capacitor voltage provides the necessary enhancement voltage to turn on the high-side switch.

Thermal Shutdown Protection

The FP6193 features integrated thermal shutdown protection. When the IC junction temperature exceeds +150°C, thermal shutdown protection will be triggered. The internal power MOSFET is then turned off to limit the device power dissipation (P_D). Once thermal shutdown occurs, this device can go back to normal operation until the junction temperature drops below +110°C approximately.

Application Information

Input Capacitor Selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible.

When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by

$$C_{IN} = \frac{I_O}{f \times \Delta V_{IN}} \times D(1-D)$$

Inductor Selection

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and / or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by

$$L = \frac{V_O + V_D}{I_O \gamma f}(1-D)$$

Where γ is the ripple current ratio

RMS current in inductor $\quad I_{Lrms} = I_O \sqrt{1 + \frac{\gamma^2}{12}}$

Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f \times L \times V_{IN}} \times \left(ESR + \frac{1}{8 \times f \times C_{OUT}} \right)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency.
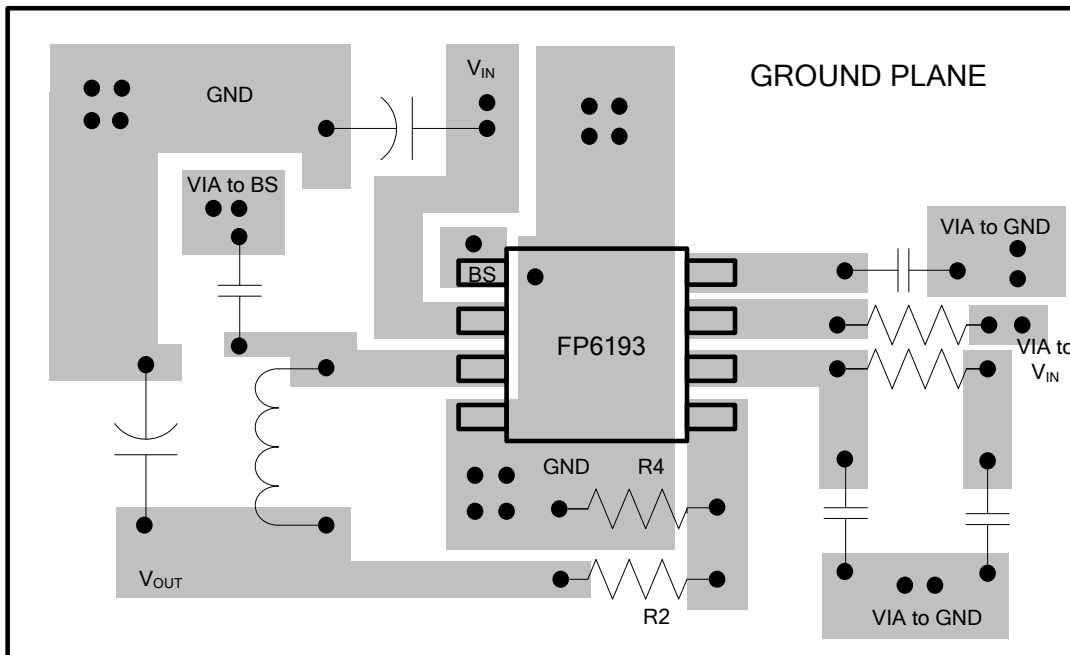
Ⅰ.In the case of ceramic capacitors

$$C_{OUT} = \frac{V_{OUT}}{8 \times f^2 \times L \times \Delta V_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Ⅱ.In the case of tantalum or electrolytic capacitors

$$ESR = \frac{\Delta V_{OUT} \times f \times L \times V_{IN}}{V_{OUT} \times (V_{IN} - V_{OUT})}$$

PC Board Layout Checklist

1. The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.
2. Place C_{IN} near IN Pin as closely as possible. To maintain input voltage steady and filter out the pulsing input current.
3. The resistive divider R_2 and R_4 must be connected to FB pin directly as closely as possible.
4. FB is a sensitive node. Please keep it away from switching node, SW. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and the layer on which the feedback trace is routed. This reduces EMI radiation on to the DC-DC converter's own voltage feedback trace.

Suggested Layout

Typical Application
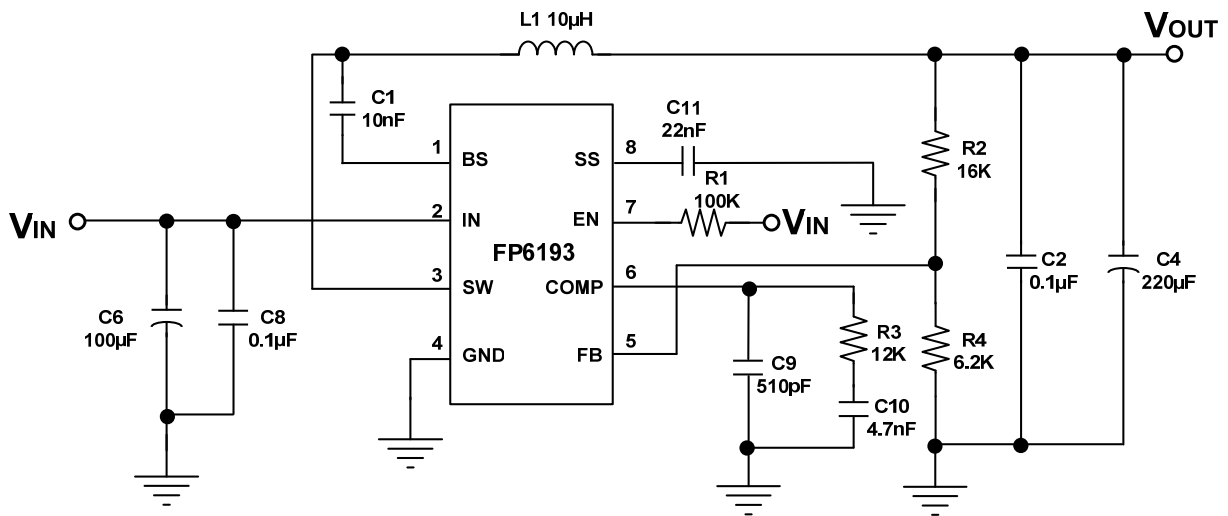
Package Outline

SOP-8L (EP)
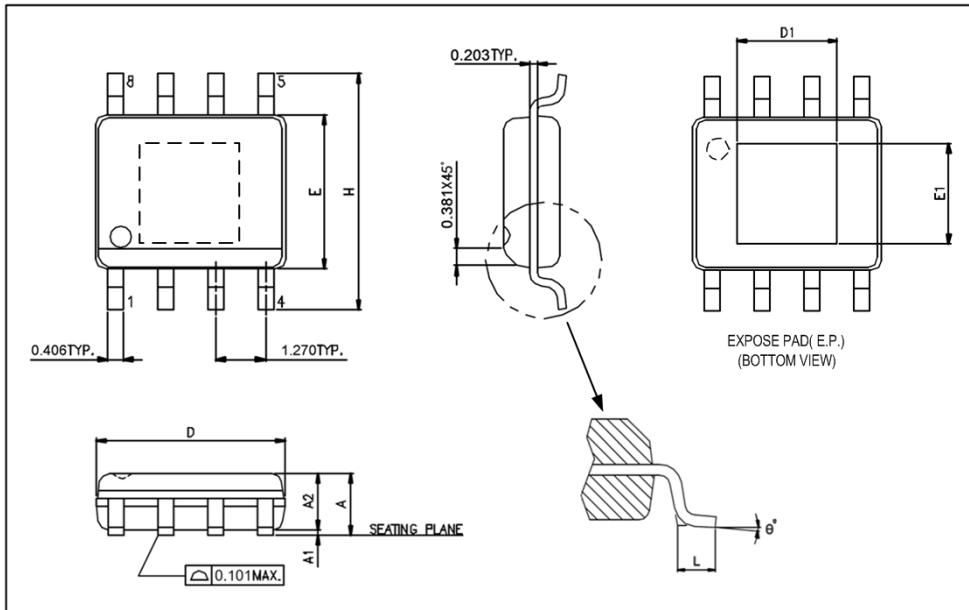
UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.050	0.152
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E1	2.184 REF	
D1	2.971 REF	

Note:

1. Package dimensions are in compliance with JEDEC Outline: MS-012AA.

2. Dimension "D" does not include molding flash, protrusions gate burrs.

3. Dimension "E" does not include inter-lead flash, or protrusions.

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